A Digitizer System for the Tile Calorimeter

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1. Overview

This note is intended to describe the requirements for the Tile Calorimeter digitizer system and to present possible designs. Several updates may be necessary to reach a fully satisfactory description. To help make the description more self-contained some additional background information is included.

The timetable outlined in the Tile Calorimeter TDR calls for mass production to begin in mid-1999. To achieve this, a prototype digitizing system must be tested in the ATLAS testbeam in the summer of 1998.

There are different design alternatives depending on some fairly independent design choices. One of those is the choice of signal compression scheme, whether to use a piece-wise linear compressor or a bilinear approach with two separate high and low gain channels. The second design choice concerns which pipeline memory solution to use, and a third which concerns the construction method to be used for the final design. Most of these alternatives can be assembled from suitable commercial ADCs, pipelines and derandomizer chips, using programmable logic to implement the readout controller function.

2. Background Information

The analog signals from the tilecal photomultiplier tubes must be digitized every 25 ns. For bunch crossings satisfying the LVL1 trigger, a group of at least 7 time slices, centered on the crossing in question must be transferred to the read out driver (ROD) system, together with the corresponding bunch crossing identifier. Since the front-end modules should be designed for maximum LVL1 trigger latency of 2.5 μs, the readout pipeline must be able to hold data for this time. This corresponds to the requirement of at least 100 pipeline slots at the given bunch crossing separation.

The system must have an overall dynamic range of 16 bits. It has been proposed to achieve this using commercial 12-bit ADCs operating at 40 M samples/sec, which is the best performance available for a reasonable cost.

The digitizing electronics will be mounted on the water-cooled cast aluminum drawer structure containing the PMTs and associated electronics. Drawers for the tilecal barrel modules contain 46 PMTs while drawers for the extended barrel modules contain 32 PMTs. The system must operate in a radiation environment corresponding to a total dose of ~10 Gy (1 kRad) accumulated in 10 years of LHC operation at design luminosity. While this is not a large dose, the electronics must nevertheless be radiation tolerant and satisfy the general ATLAS requirements outlined in Ref. [1]. In particular, tests of the system must be performed in a radiation environment before mass production begins.

The relative timing of the PMT signals vary over the length of a drawer due to time-of-flight effects and the differing lengths of the optical fibers to the PMTs. For the barrel drawers the time variation between the fastest and slowest signals is ~5 ns, and for the extended barrel drawers it is ~9 ns. It is desirable to have one digitization within a few ns of the peak of the analog input signal. This reduces sensitivity to time jitter in the digitizing clock, and eases subsequent processing of the samples. This can be realized by local adjustments of the clock phase.

It is intended that each tilecal module be largely self-contained, with its electronics drawer installed prior to test beam calibration and/or calorimeter assembly. There should be a minimum of connections between each electronics drawer and the outside world.

The LVL1 trigger information from tilecal is in the form of a fast analog pulse with an amplitude proportional to the sum of the 5 PMT signals in a calorimeter tower. This pulse is transmitted to the LVL1 trigger electronics, where sets of 6-8 digital samples are taken and processed to obtain bunch crossing identifications and corresponding energy estimates. No trigger information is required from the tilecal digitizing system itself.

The output of the digitizing system is transferred from the drawers to the ROD system where the signal from each calorimeter cell is corrected for calibration effects. Bunch crossing identification is done on the cell signals and a best estimate is made of the energy in each cell. This is similar to the procedure for the liquid Argon electromagnetic calorimeter.

The overall requirements for the tilecal readout are summarized in Table 1. These are based on a calorimeter light yield of 50 photoelectrons/GeV/cell and a photomultiplier gain of 10^5.

Quantity	Compr Option	Bi-linear Option	
		Low Gain Chn	High Gain Chn
Maximum energy / cal. cell	2 TeV	2 TeV	2 TeV
Maximum energy / readout chn	1000 GeV	1000 GeV	63 GeV
Maximum charge / readout chn	800 pC	800 pC	50 pC
Dynamic range	16 bits	12 bits	12 bits
LSB (energy)	15 MeV	244 MeV	15 MeV
LSB (voltage for 1 V full scale)	15 μV	244 μV	244 μV
Muon energy / cal. cell	350 MeV	350 MeV	350 MeV
Muon counts / readout chn	11	0.7	11

3. Digitizer Input Signals

(a) Analog Signals

The analog input to the digitizing system is produced by a charge sensitive pulse shaper circuit located on the 3-in-1 electronics board in each PMT block. Unipolar differential analog signals are produced and transmitted to the digitizing electronics on shielded cables.

As noted above, two alternative types of input analog signals have been proposed to achieve a dynamic range of 16 bits. In the first scheme, the analog signals are processed by a non-linear range compressing amplifier. This yields an AC coupled differential output signal with 12 (or possibly 10) bits dynamic range. In the second scheme, two linear differential signals are produced with a gain ratio of 16. In the current version of this bi-linear system, each signal has a peak amplitude of ±0.5 V and the pulse shape shown in Fig. 1. The output impedance of the signals from the 3-in-1 electronics is 50Ω with respect to ground and the signals are AC coupled. The AC coupling produces a small baseline shift which is measured directly as part of the pedestal of subsequent events. The time constant of the recovery is ~100μs, so a full scale signal produces a maximum shift of ~0.5 mV (2 counts). Imperfect shaping may also lead to a small negative undershoot.

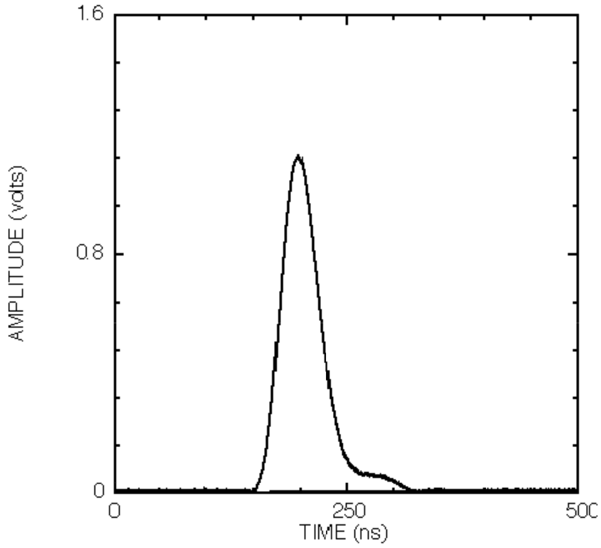

Fig 1. Output signal from the bi-gain shaper.

(b) Digital Signals

The ATLAS timing, trigger, and control (TTC) system provides control signals for the readout system. It is the source of the 40.08 MHz bunch crossing clock used for digitizing the analog data. It provides a synchronous LVL1 accept signal for bunch crossings with data to be recorded, a 12-bit bunch crossing identifier to label the associated data and a 24-bit event number. Finally, it can provide receiver-specific data for controlling the readout system. A custom TTC receiver chip (TTCrx), developed by J. Christiansen et al., is intended for use in front-end digitizing systems[2].

The TTCrx chip produces two 40.08 MHz clock outputs, whose timing with respect to the bunch crossing clock can be varied in steps of 104 ps from 0 to 25 ns. The arrival of the LVL1 accept signal, and the associated bunch crossing identifier can be adjusted by up to 16 bunch crossings to compensate for propagation delays.

It is expected that the ROD electronics will also use a TTCrx chip and will therefore be able to append the 24-bit event number to the data. Thus the data from the drawer will only contain the bunch crossing identifier.

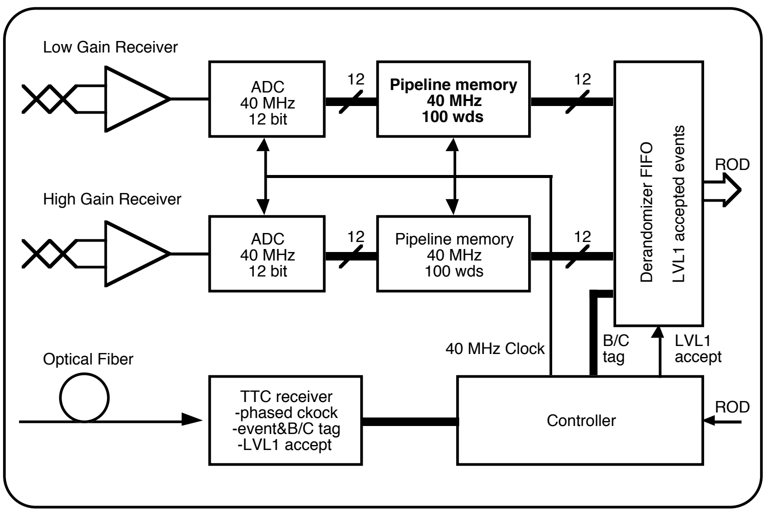

Fig 2. A schematic overview

4. Digitizer operation

The analog input signals are digitized at the system clock frequency and fed continuously to the pipeline memories. Each first level trigger accept will cause a programmable sequence of samples around the event to be written to a derandomizing buffer. There should be a sufficient number of such buffers to limit the risk for overrun (about 5). The stated maximum latency of 2.5 μs can be accommodated by using pipeline memories with a depth of 100 time slots. Each time frame should be sufficiently large to contain enough samples to cover most of the 200 ns pulse and sample the pedestal. A maximum of 15 samples may be desired, although the most probable size is about 7. It is furthermore desirable that the derandomizer function is designed so that overlapping time frames are read out independently disregarding the redundancy of reading out the overlapping samples several times. The buffer is then packaged together with the appropriate bunch crossing identifier and sent to the ROD.

Read-out controllers will also make certain that corresponding time frames from all channels are pushed consecutively to the RODs, subject only to ROD flow control (fig. 3). The controllers should report error conditions by setting error flags in the data stream. Each time frame should also be accompanied by a bunch crossing identifier. Implementing the design in programmable logic will allow flexibility to try different read out strategies. In the case of a bi-gain solution it will be possible to select readout of both high and low gain samples, to select the appropriate gain on a sample to sample basis or on a time frame basis. It will also be possible to vary the time frame size. In the prototype it should be possible to reprogram the controller FPGA during operation.

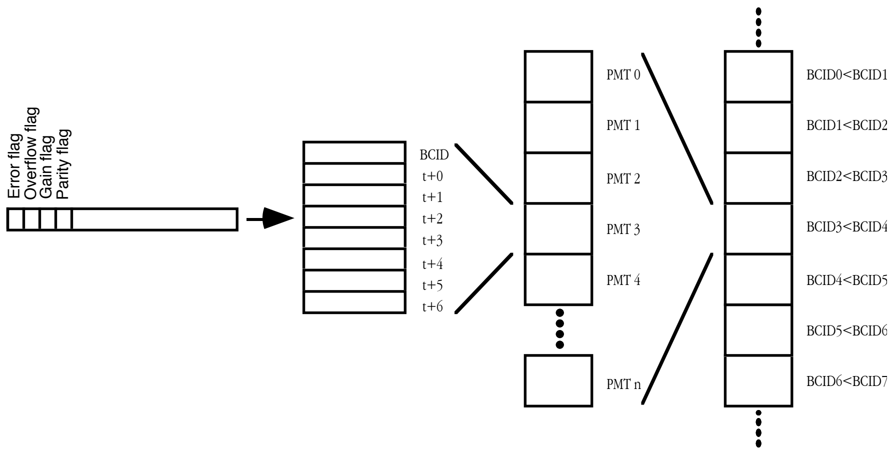

Fig 3. Data flow

5. Output Signals

The primary output from each drawer is the digital data to the ROD modules, which will be transmitted using the S-link protocol [3], as proposed by the Valencia group. Using the 32 bit S-link option will allow the transfer of two simultaneous channels with range flags, overflow flags, and error flags. The remaining two bits may be used for parity protection. According to specifications, S-link will now allow 32-bit transfers at a rate of up to 40 MHz. Whether this rate can be sustained depend on the performance of the receiving end. If the receiver is located in a PCI bus the average rate will not exceed 33 MHz. With a level 1 accept rate of 100 kHz and transfer rate of 40 MHz the maximum frame size will be 16 ≈ (40x2x10)/48. 33 MHz will limit the frame size to 13.

It is noted that the initial ATLAS specification for the LVL1 accept rate is 75 KHz but this must be upgradable to 100 KHz at a future date. Since it will be difficult to modify the drawer electronics, an initial specification of 100 KHz is retained. The reduced LVL1 accept rate could have an impact on the ROD modules.

6. Design Considerations

The system require 12-bit ADCs operating at 40 M samples/sec. Several companies market such AD converters with varying performance, precision, latency, power, and prices. Potential vendors include Analog Devices, Burr-Brown, and National Semiconductor.

Awaiting in the pipeline up to 100 clock periods, events passing the LVL1 trigger must enter a derandomizing buffer on each channel to permit transfer to the ROD modules at 100 Kevents/sec without data loss. Some suitable pipeline chips are available such as TEC-DMU [4] from SiCon and the FERMI channel chip. The former was designed for use in the PHENIX heavy ion experiment at RHIC. It has been in the market for one year and has been tested extensively. It contains a pipeline of variable length, up to 190 time slices. The time frame length is also programmable, up to 80 samples. It has 5 independent derandomizer buffers. The data width is 24 bits which will allow two channels per buffer, but without room for accompanying error or data integrity bits. Furthermore it does not include bunch crossing identification, which will make it difficult to detect if a derandomizer looses synchronization. The present TEC-DMU is also implemented in a standard process, without built-in fault tolerance. The FERMI channel chip contains 5 derandomizer buffers and a pipeline up to 256 deep with a 12 bits data width. It is also implemented in a standard process but does contain a considerable number of error detection facilities. A third alternative to use dual port memories with a dedicated memory controller (address generator) for each group of 12 channels. Such a design was investigated in RD-16 [5, 6]. A memory controller for the Tile Calorimeter readout can easily be implemented in a FPGA circuit, which may even contain the pipeline and the derandomizer themselves.

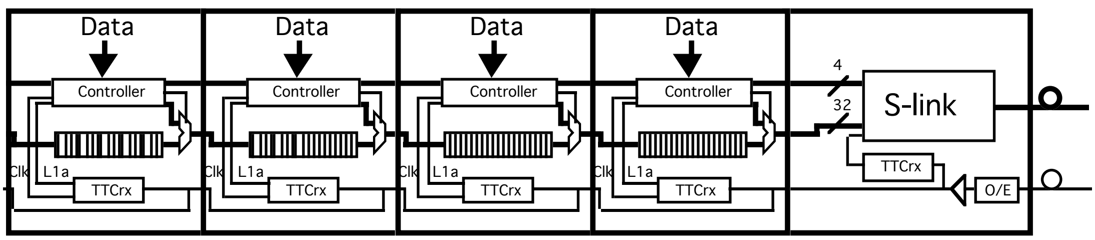

Fig 4. Partitioning of the barrel readout into four boards with an S-link connection to the ROD system

7. Outline of a Possible Configuration

A suitable partitioning of the digitizing system is to build modules which services 12 channels each. This means that four identical boards will read out the 46 channels of the barrel drawers, while three would be needed for the extended barrel. It is possible to design the boards so that they only require connections with their immediate neighbors (fig. 4). During the first phase of read-out the multiplexer will transmit data from the controllers while the input data fill the by-pass FIFO. The last board will be connected directly to a specially designed S-LINK transmitter (LSC) board, which is in turn connected to the ROD, to be designed by the Valencia group. The return lines will be used to control the operation of the digitizers and to program its controller FPGAs. This S-LINK board will also receive and distribute (electrically) the system fiber containing clock and the level 1 accept signal. The digitizer board design will not be trivial, since it will contain both analog signals with 12 bit dynamic range and high speed digital signals. Then the multiplexer switches to take data from the pipeline memory which now forms a large shift register. This will require a careful board layout with separate power and ground planes as well as impedance matched lines in sensitive areas.

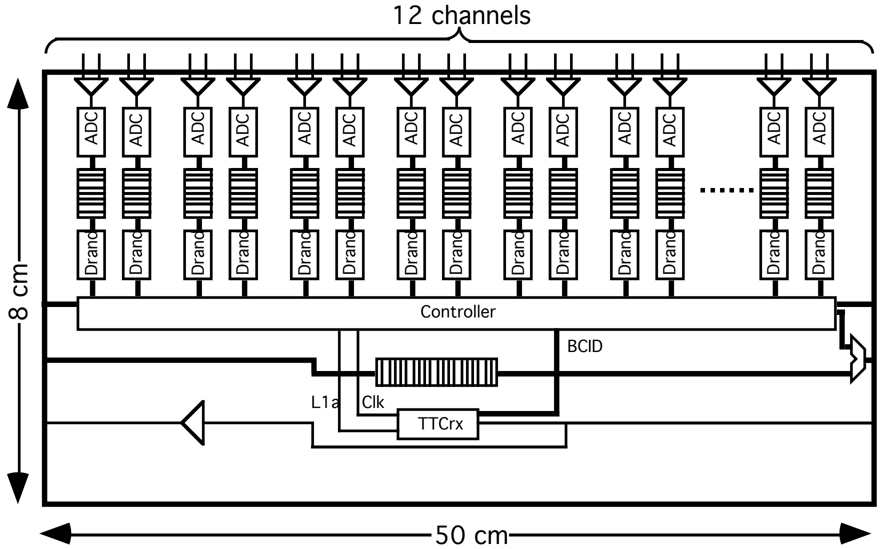

Fig 5. A possible digitizer module design

One possible plan is to distribute the digitizing electronics over the full length of the drawer. This leads to much shorter cables between the 3-in-1 cards and the ADCs, and is possible because grouping of the digitizers into trigger towers is no longer needed. One might consider a digitizer board approximately 50 cm long, able to digitize the signals from 12 PMT channels

Since each TTCrx chip produces two bunch crossing clocks with independently adjustable timing, all signals can be sampled within ~1 ns of the peak of the pulse.

8. Prototype Development

Several questions must be resolved before the optimal design can be chosen for production. However, it is essential to build a functional demonstrator which fits into the drawers in the 1998 tests and is a candidate to the final design. This prototype will probably use the TEC-DMU chips described above. These can be connected to an FPGA controller which can implement the essential parts of the final protocol. It will be possible to reprogram the FPGA at any point so that different readout protocols may be investigated. The boards will also contain the TTCrx chip. During the initial beam tests the chain of boards will connect via S-link to a VME motherboard in the DAQ system. The TEC-DMU system may not fill all the data integrity and radiation tolerance requirements. To determine the reliability and radiation tolerance of the option chosen will be one of the goals of the system tests. If these requirements are not met, suitable modifications will be needed.

9. The Final System Design

For the final design it will be possible to use different construction methods. The demonstrator will be a circuit board with mostly surface mounted components. Another possibility is to use separate dense modules for pairs of analog channels or larger aggregates of ADCs using the Chip-On-Board (COB) technique. It is also possible to implement these units in a Multi-Chip-Module (MCM). The optimal construction method will in this case not affect the functionality or even the circuit design. The choice can then be based on performance, radiation tolerance, reliability, cost and compatibility with the time table.

10. Time Schedule

The intention is to manufacture a first prototype as a circuit board during the fall of 1997 using the TEC-DMU pipeline chip. Prior to this, detailed VHDL simulation must be performed to verify the functionality of the digital part of the design. The TEC-DMU and the DPM solution will be compared for optimum performance. The analog front-end will have to be studied with SPICE. Since this work will be performed before the compressor choice is made (late this fall), the design will assume a bi-linear operation, which is more demanding.

It will also be necessary to design the dedicated S-LINK (LSC) board. With such a board it will be possible to receive test beam data with a standard SLINK interface connected to a PMC mother board in a VME crate.

A later step may be to design and manufacture a chip on board (COB) version. If it is functionally and size wise identical with the PCB version it will be easy to test. In parallel with this development a FERMI MCM will be tested and evaluated. The MCM and COB implementations will be compared with respect to size, noise, system cost and reliability.

11. Design Procedures

A top down design approach will be followed, where a rather clear and complete description of the system will be developed before detailed design begins. Vendor quotes will be obtained for the principal ICs before being included into the design.

The design details will be developed and agreed to by the Chicago, Stockholm and Valencia groups, following adequate discussion. The proposed plan will be presented to the rest of the Tile Calorimeter community before being finalized.

References

1. ATLAS requirements on radiation tolerance,
http://nicewww.cern.ch/~FARTHOUA/FEWWW/radhard.html

2. J. Christiansen et al., TTCrx Reference Manual, Version 2.2,
http://pcvlsi5.cern.ch:80/MicDig/ttc/MANUAL22.PDF

3. Specifications and current implementations of the CERN S-link system,
http://www.cern.ch/HSI/s-link/

4. http://www.sicon.se/products.html

5 FERMI note # 5 G. Appelqvist and C. Bohm: "A memory controller for FERMI", November 1991

6. FERMI note # 22 A. Savoy - Navarro et al. " The Memory controller", August 1993