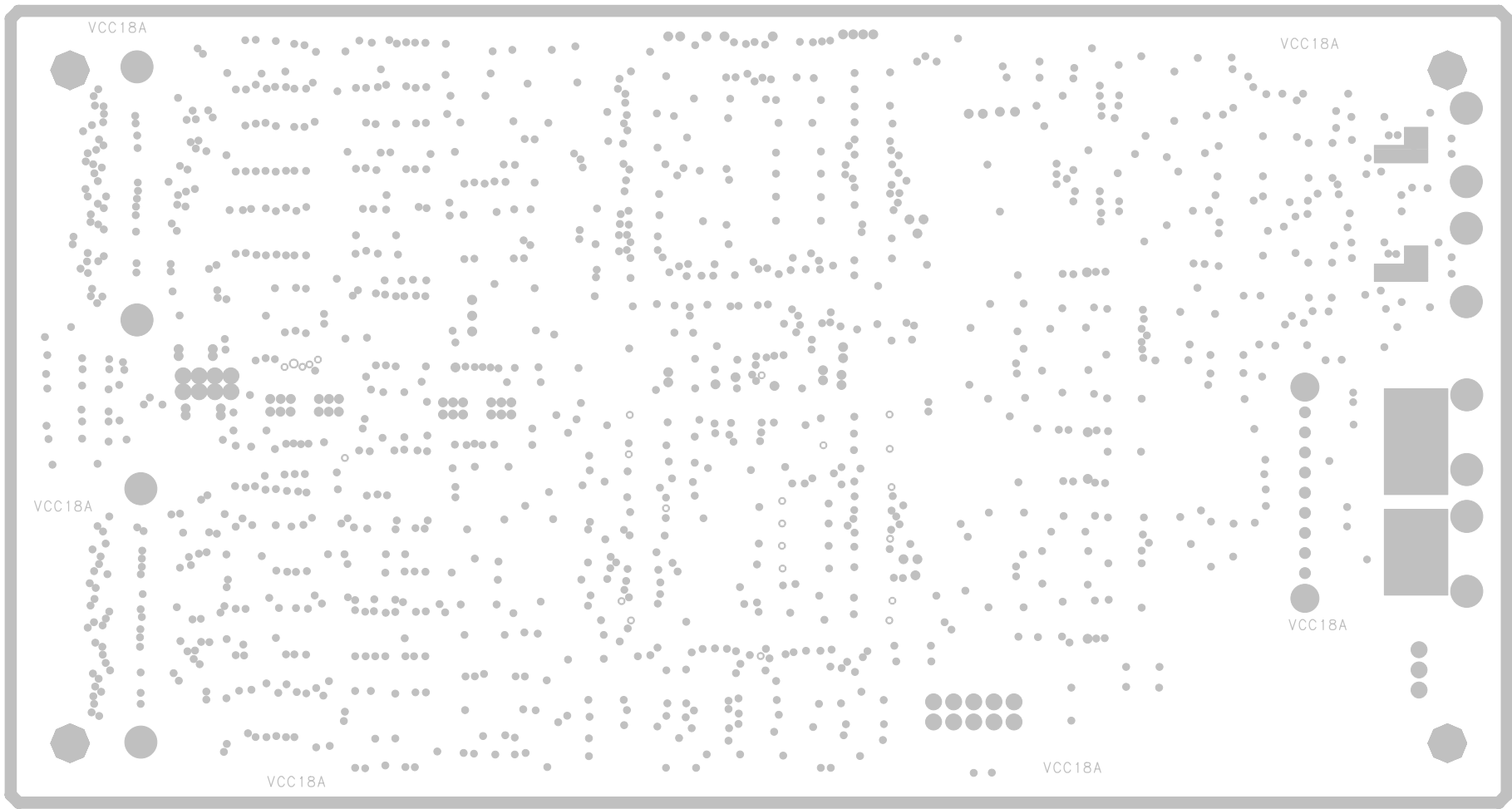
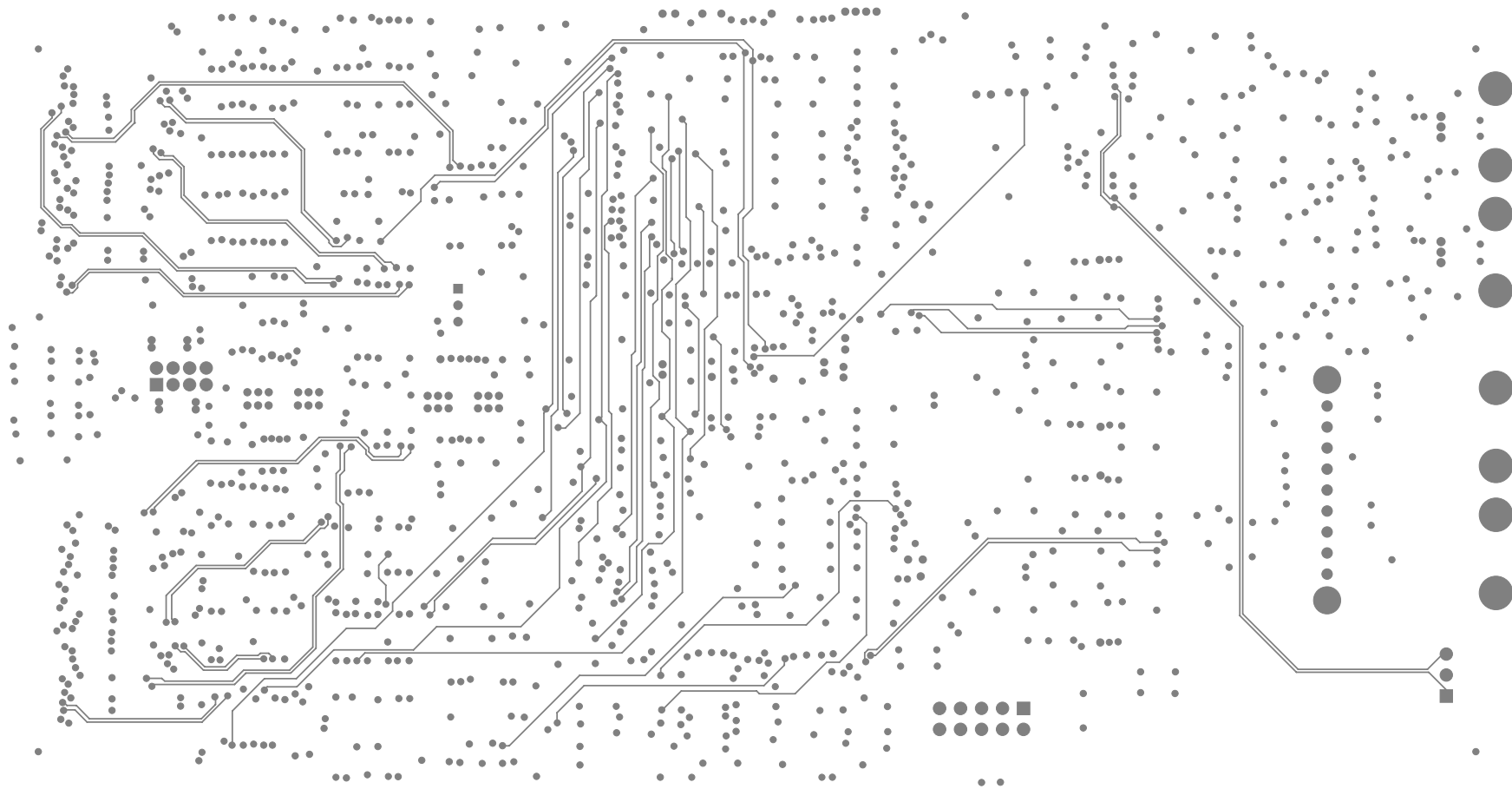


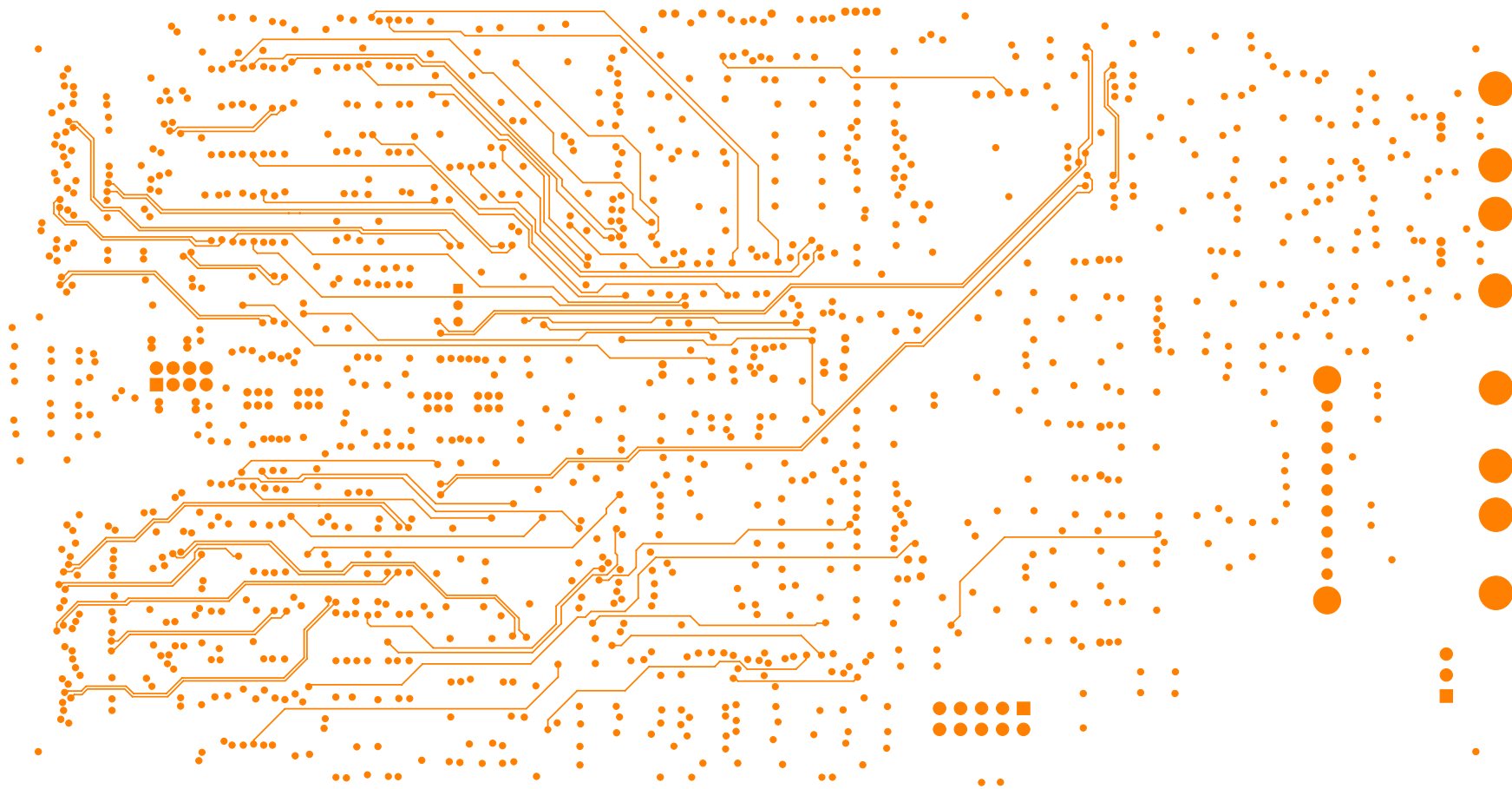
Artwork_1: Top Component Layer (SIGNAL_1)



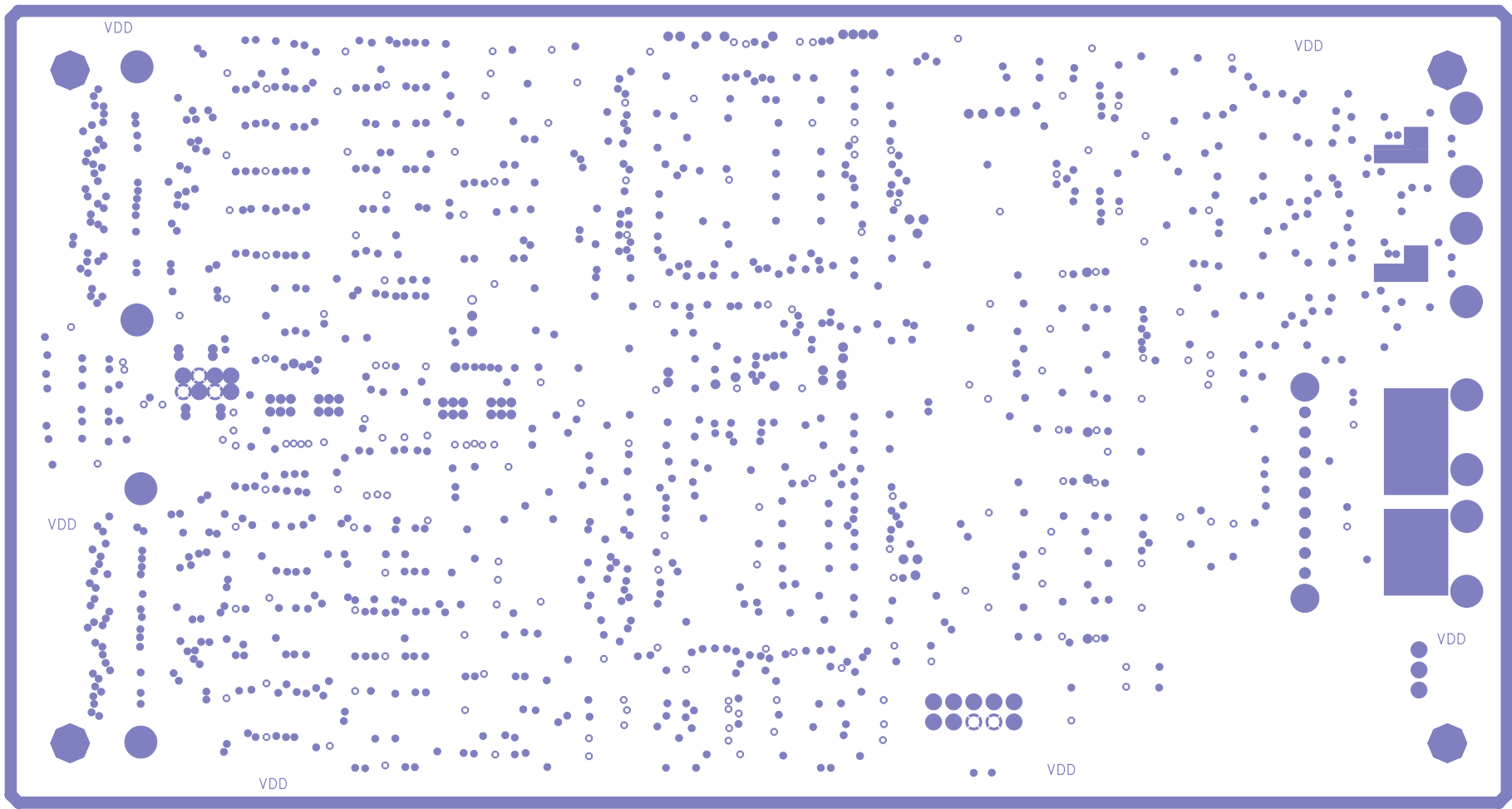
Artwork_2: Power_2 (VCC18A)



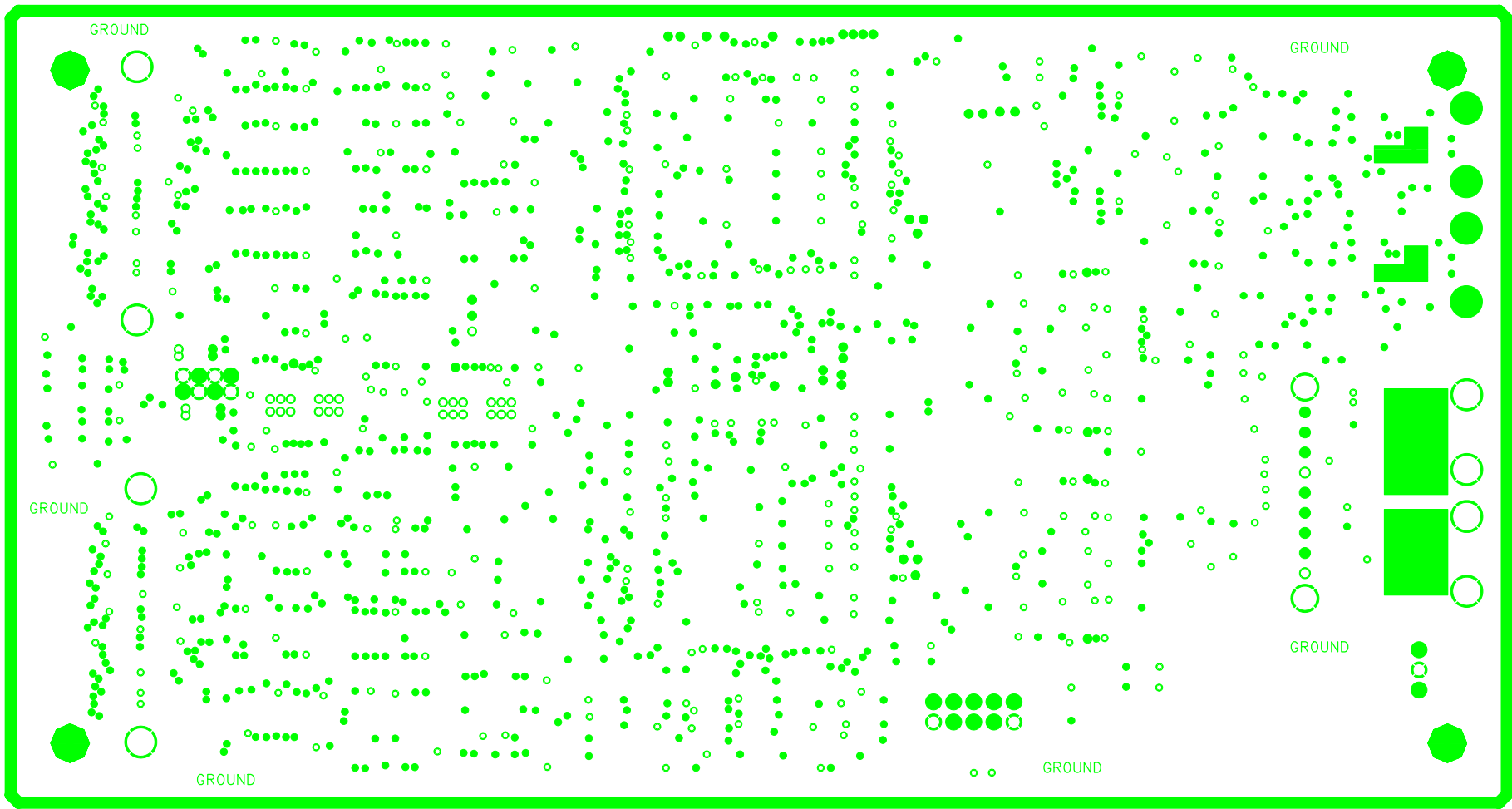
Artwork_3: Inner Signal layer (SIGNAL_2)



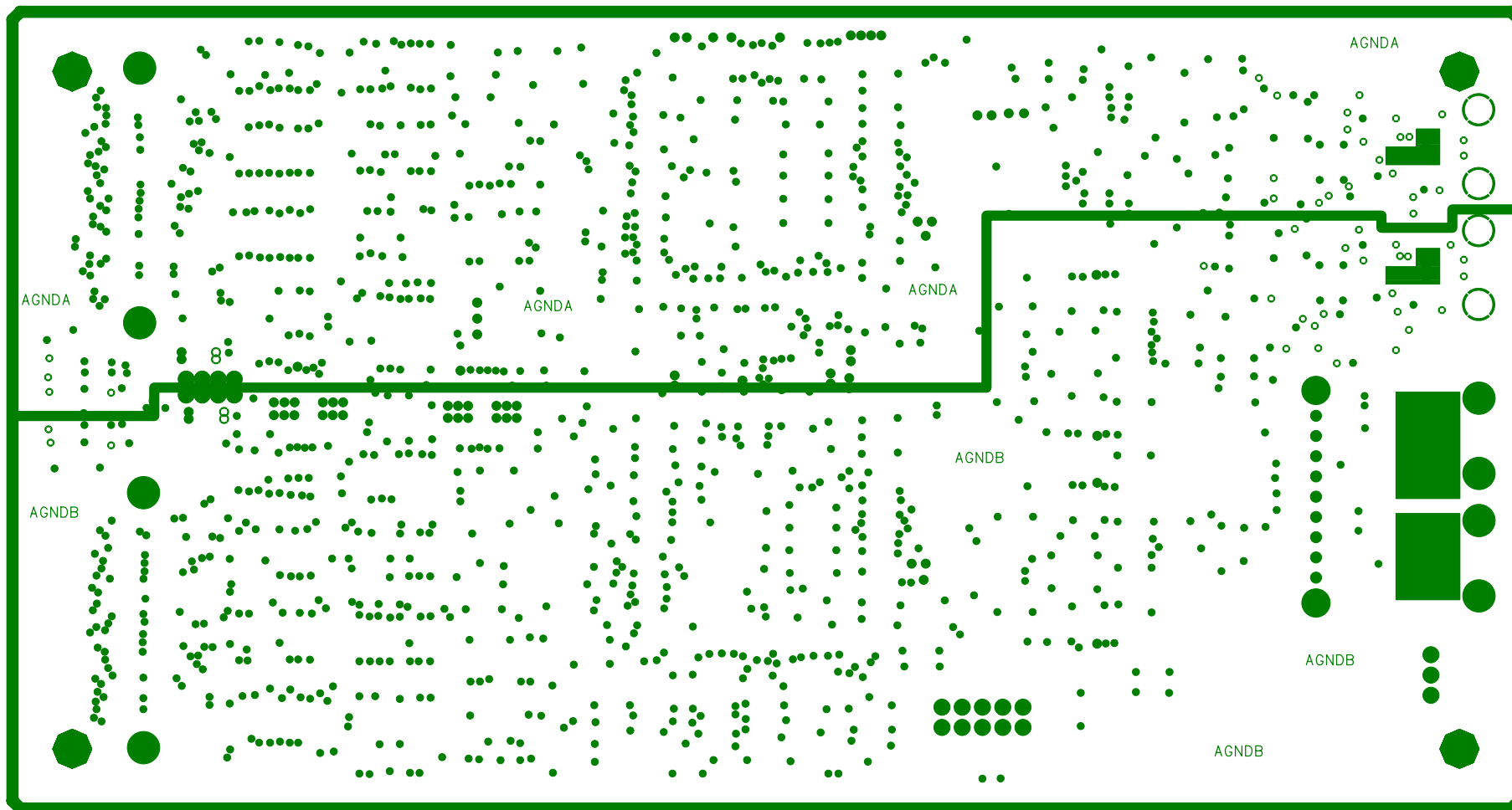
Artwork_4: Inner Signal Layer (SIGNAL_3)



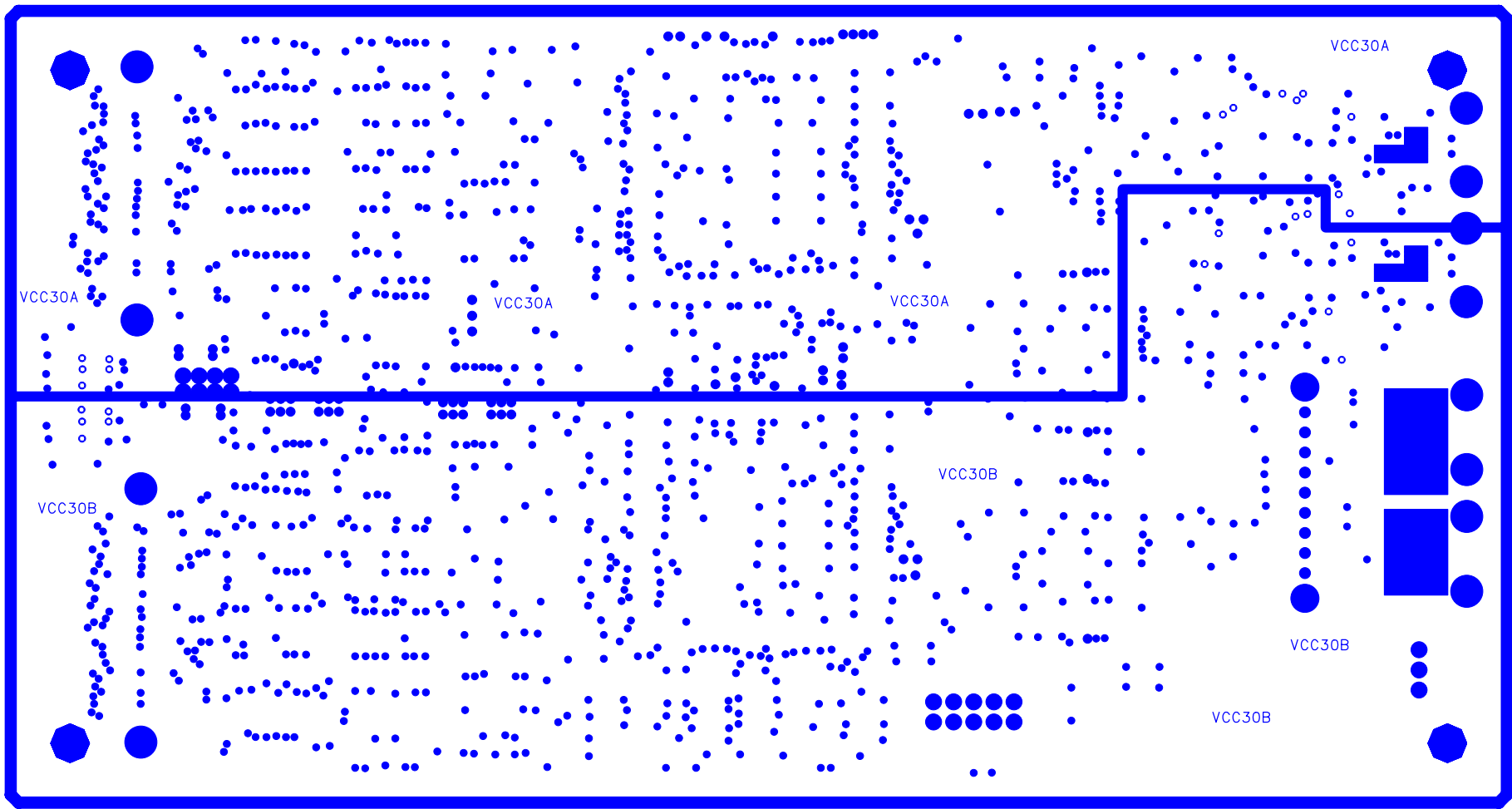
Artwork_5: Power_4(VDD)



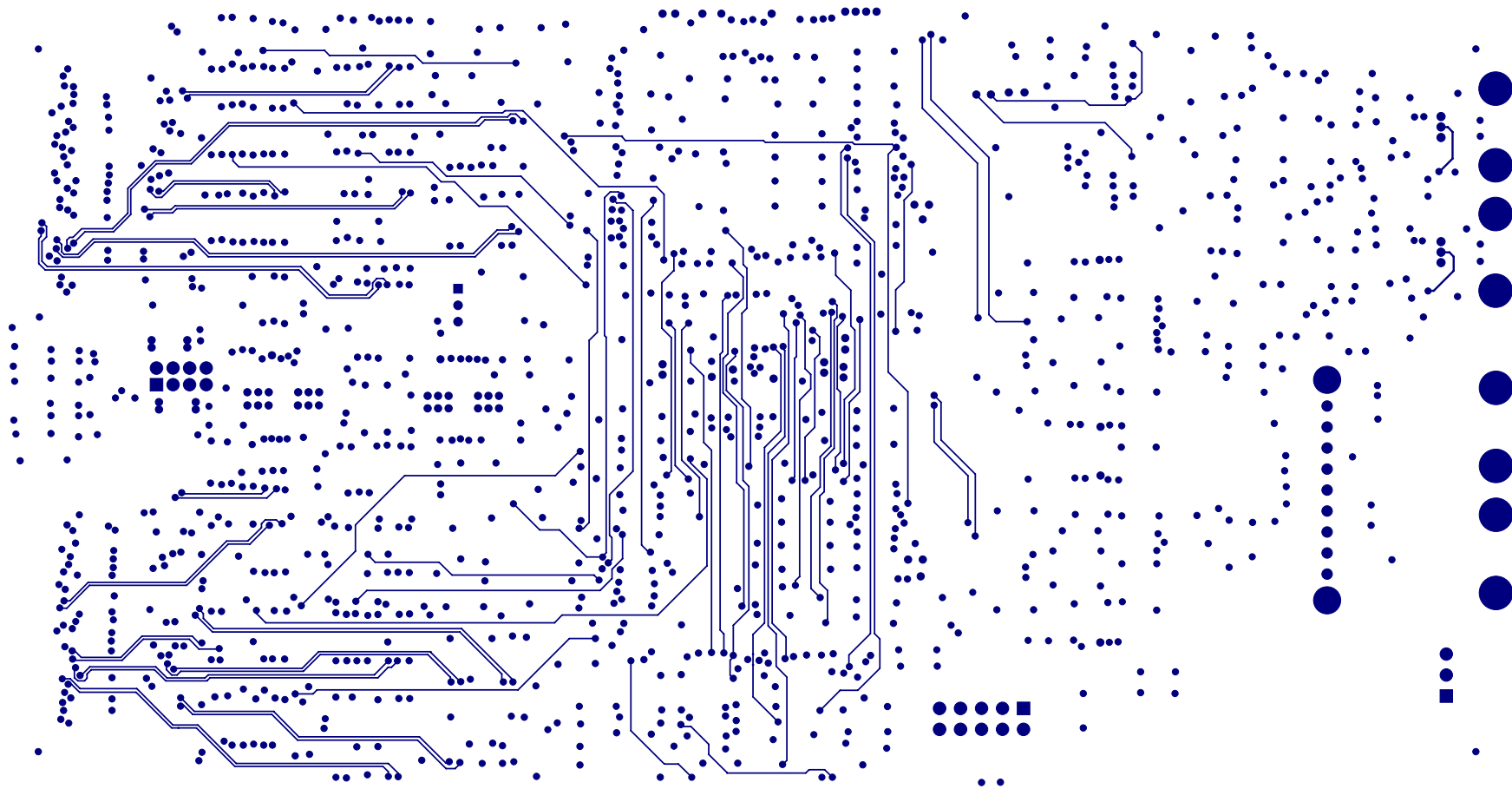
Artwork_6: Power_1 (Ground)



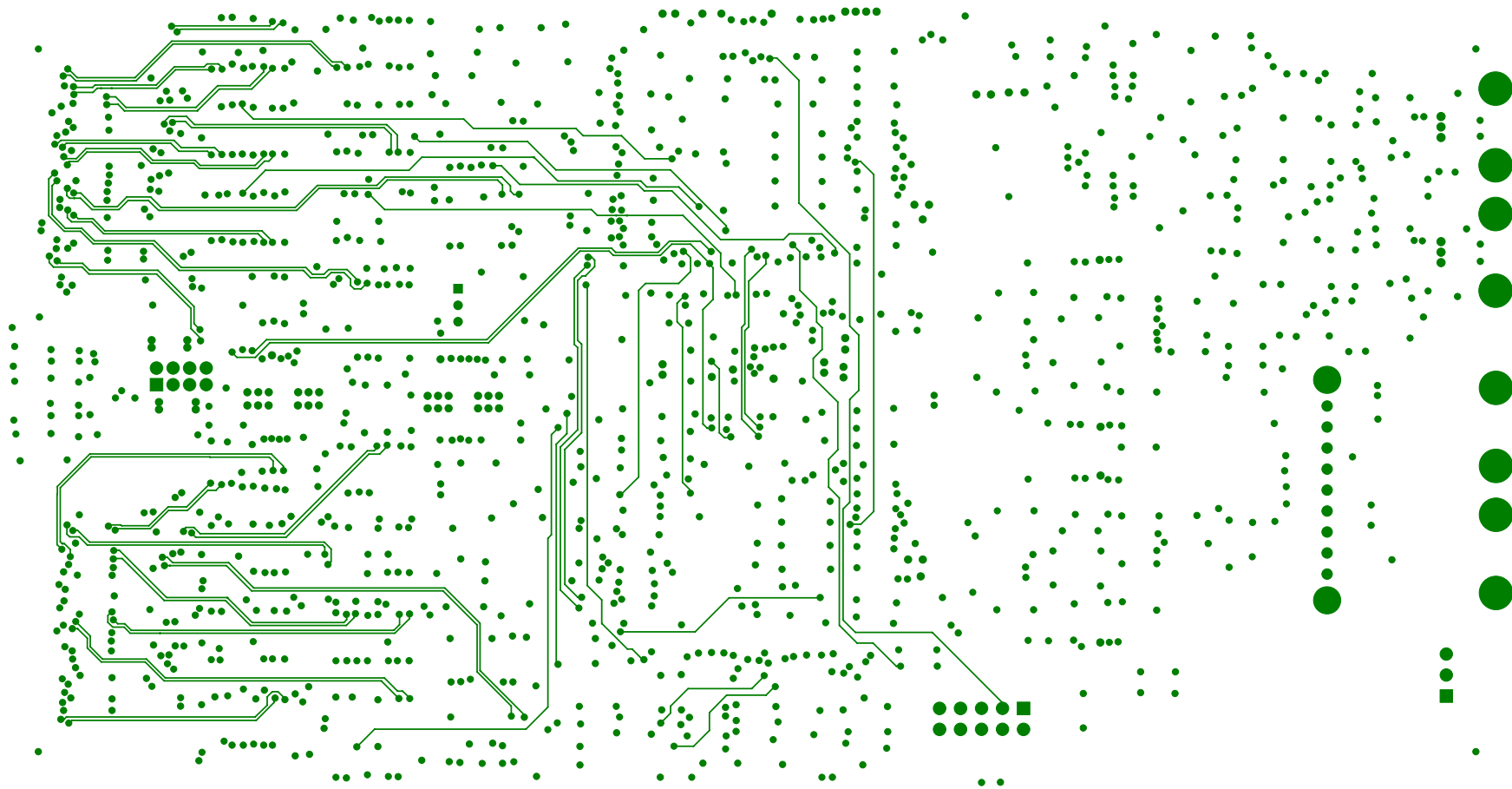
Artwork_7: Splited power plane(AGNDA, AGNDB)



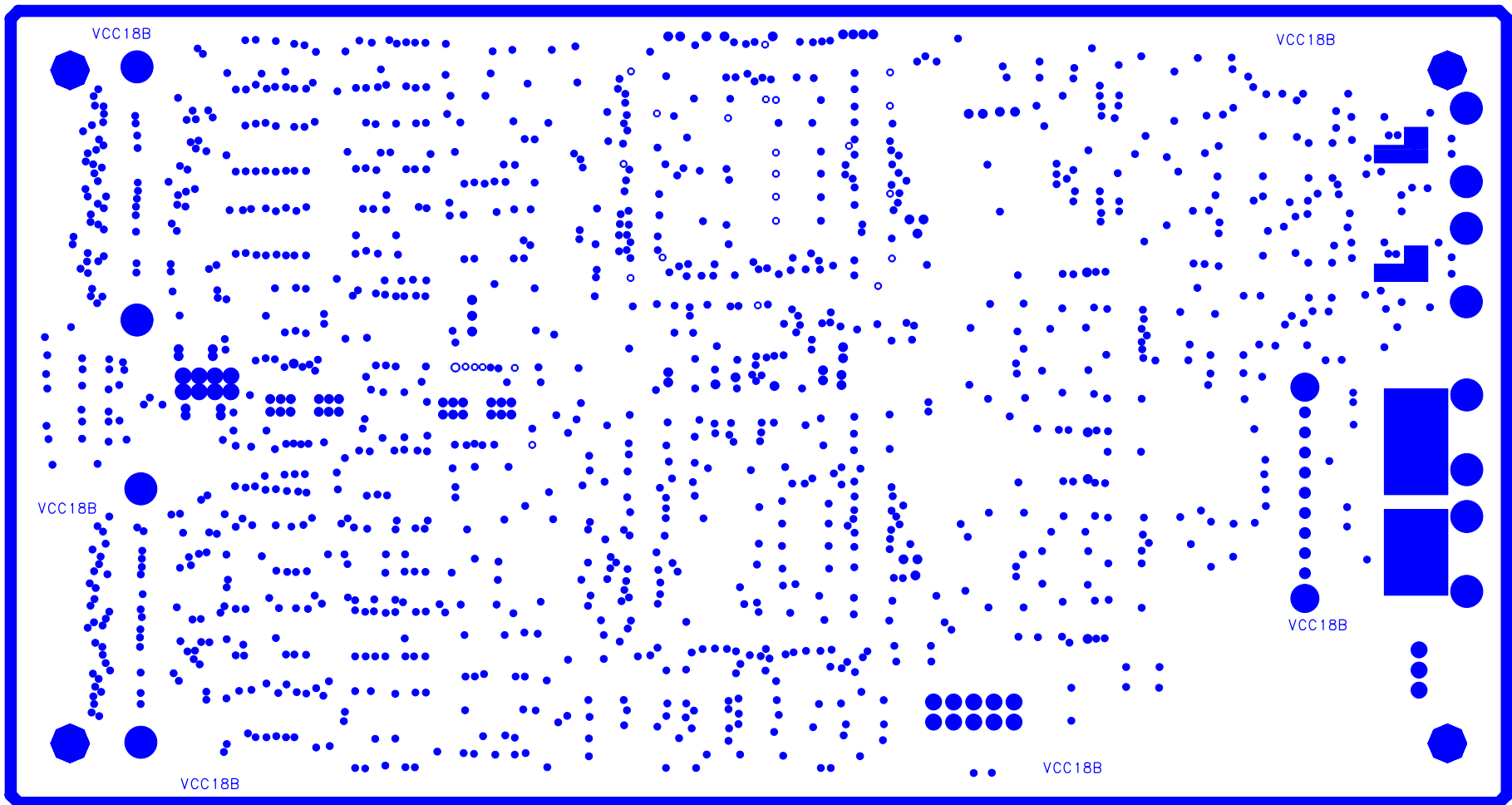
Artwork_8: Splited power plane(VCC30A, VCC30B)



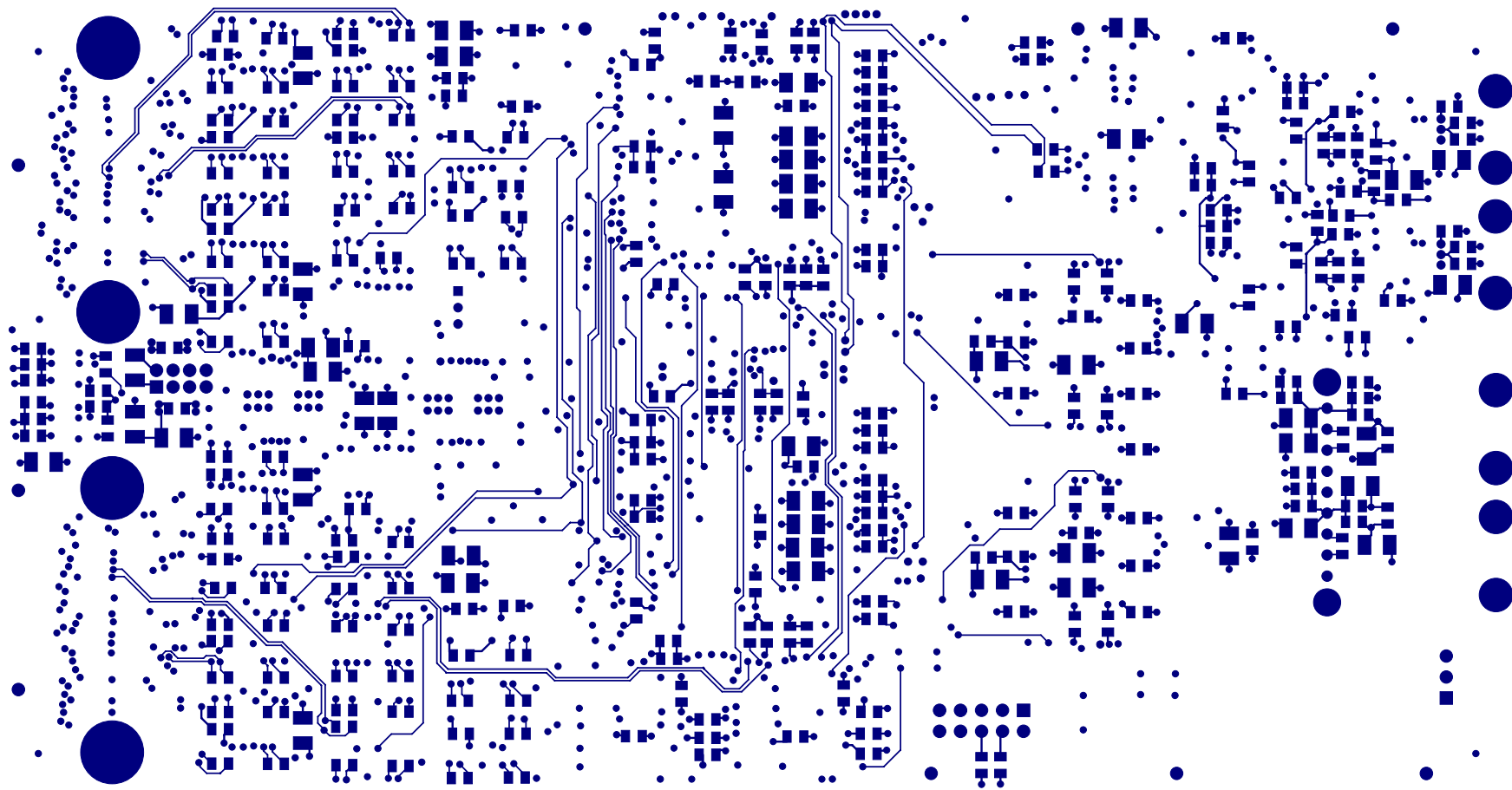
Artwork_9: Inner Signal Layer(SIGNAL_4)



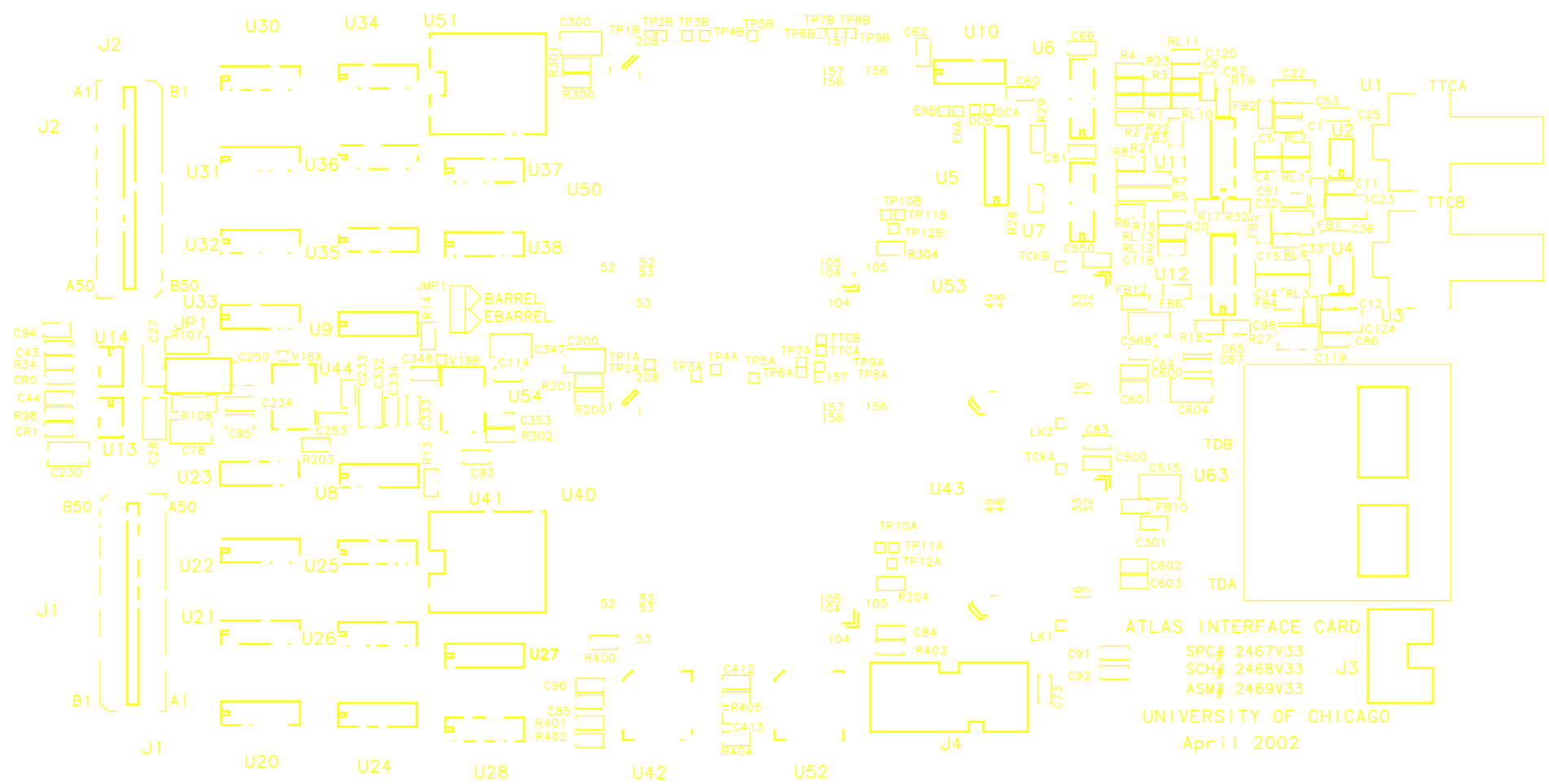
Artwork_10: Inner Signal Layer (SIGNAL_5)



Artwork_11: Power_3 (VCC18B)



Artwork_12: Bottom component layer (SIGNAL_6)



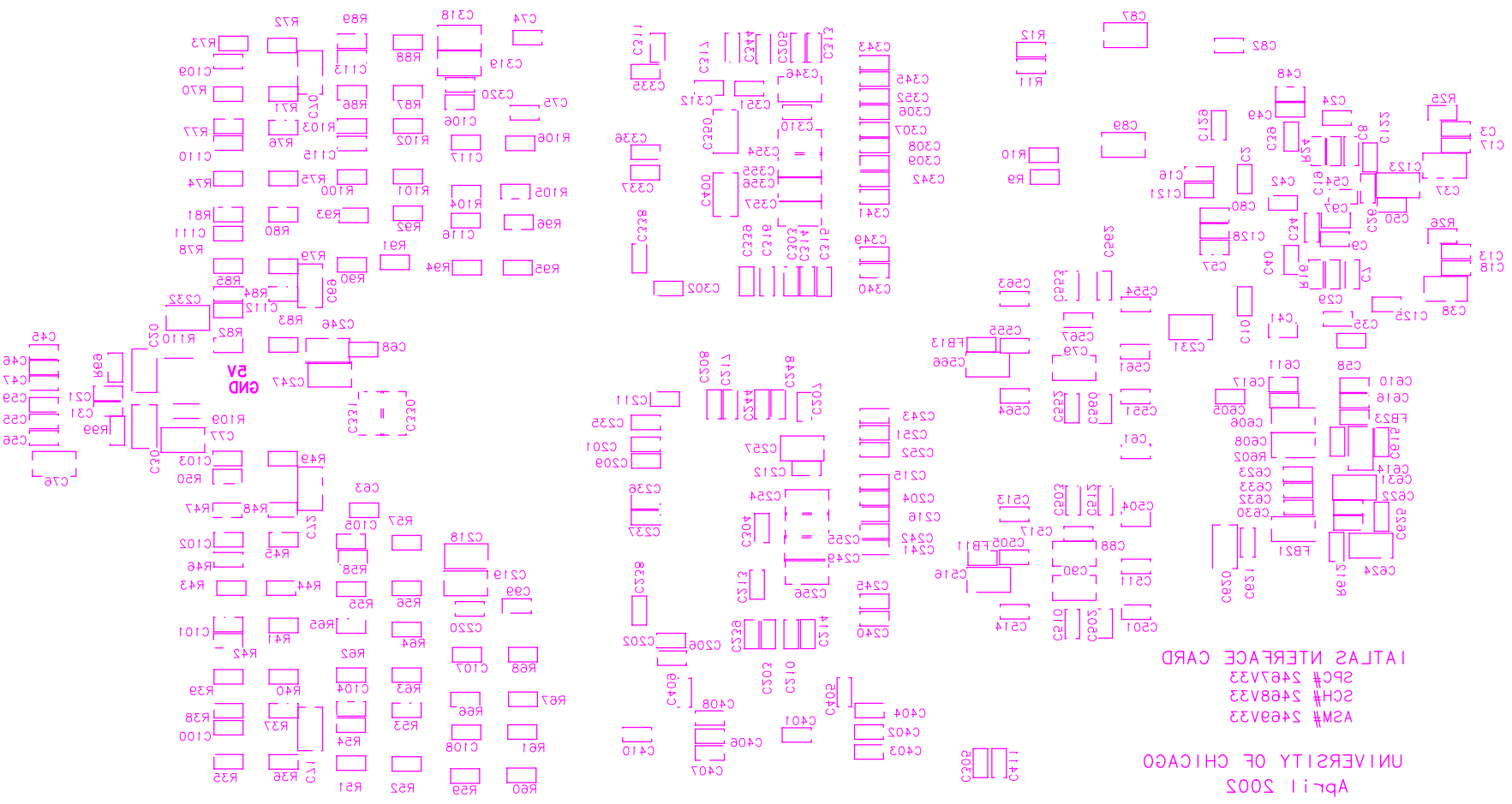
ATLAS INTERFACE CARD
SPC# 2467V33
SCH# 2468V33 J3
ASM# 2469V33
UNIVERSITY OF CHICAGO
April 2002

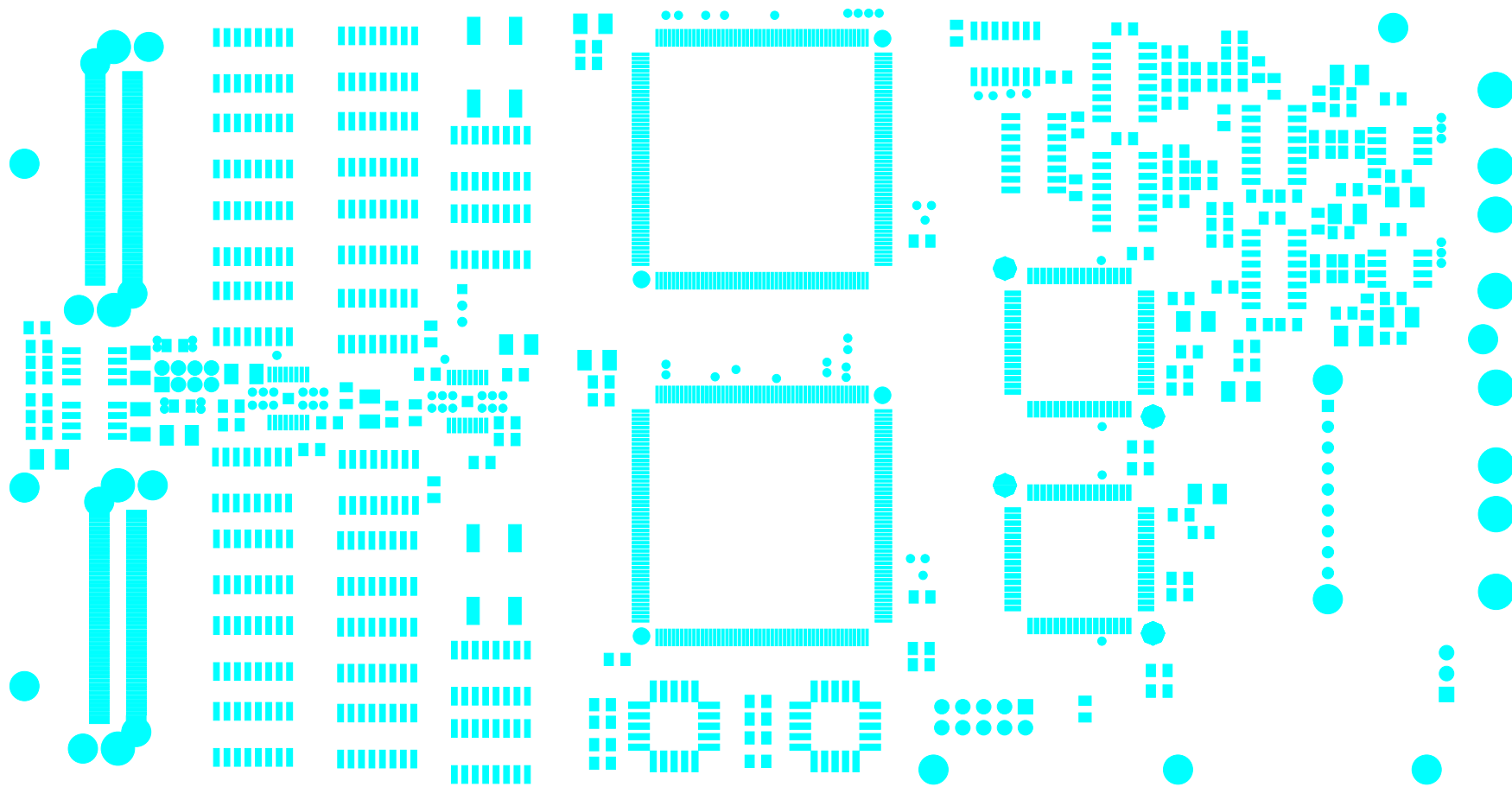
Artwork_13: Top silkscreen



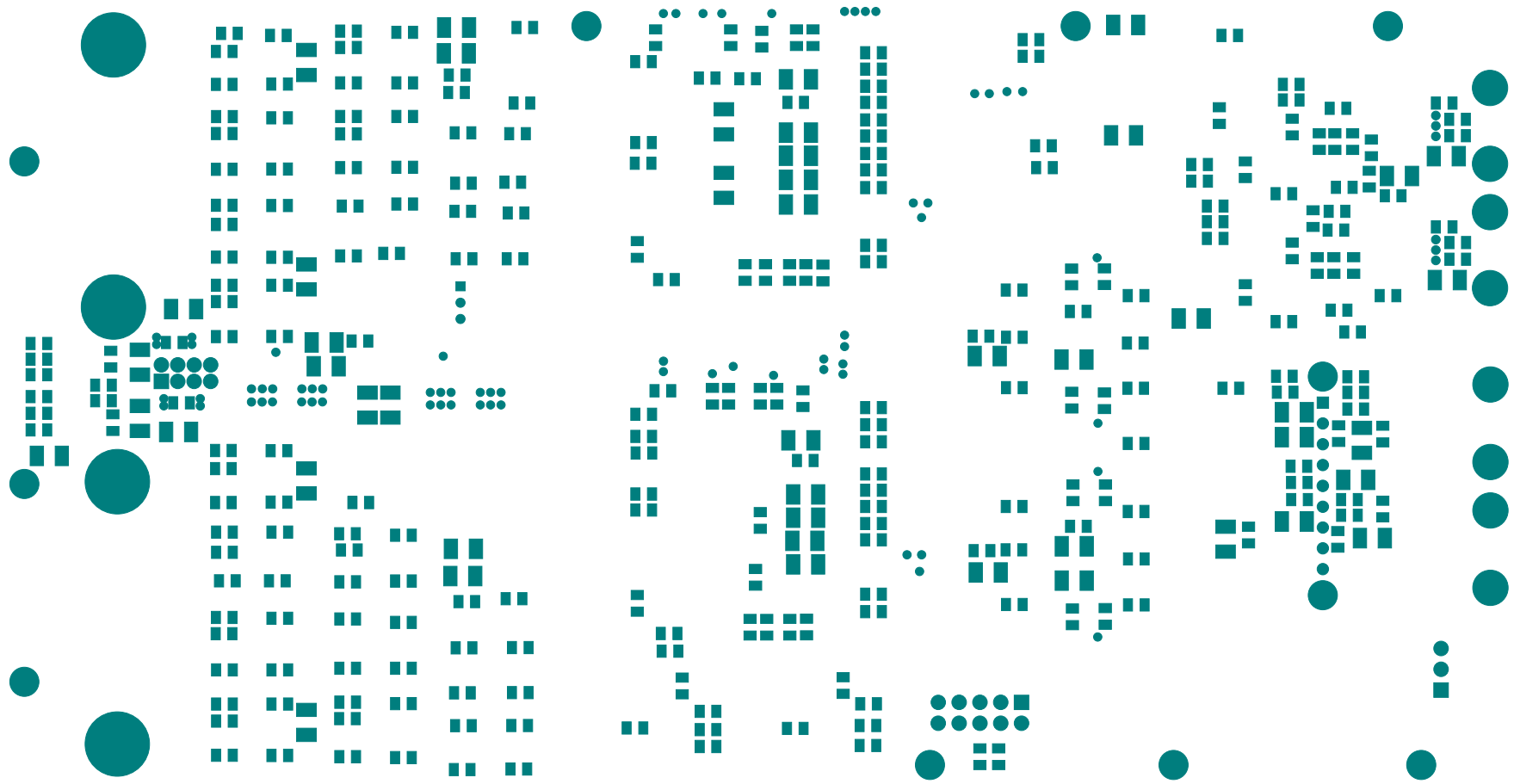
Artwork_14: Bottom silkscreen

April 2002
UNIVERSITY OF CHICAGO
ASM# 246A33
SCH# 246A33
SPC# 246A33
LATAS INTERFACE CARD

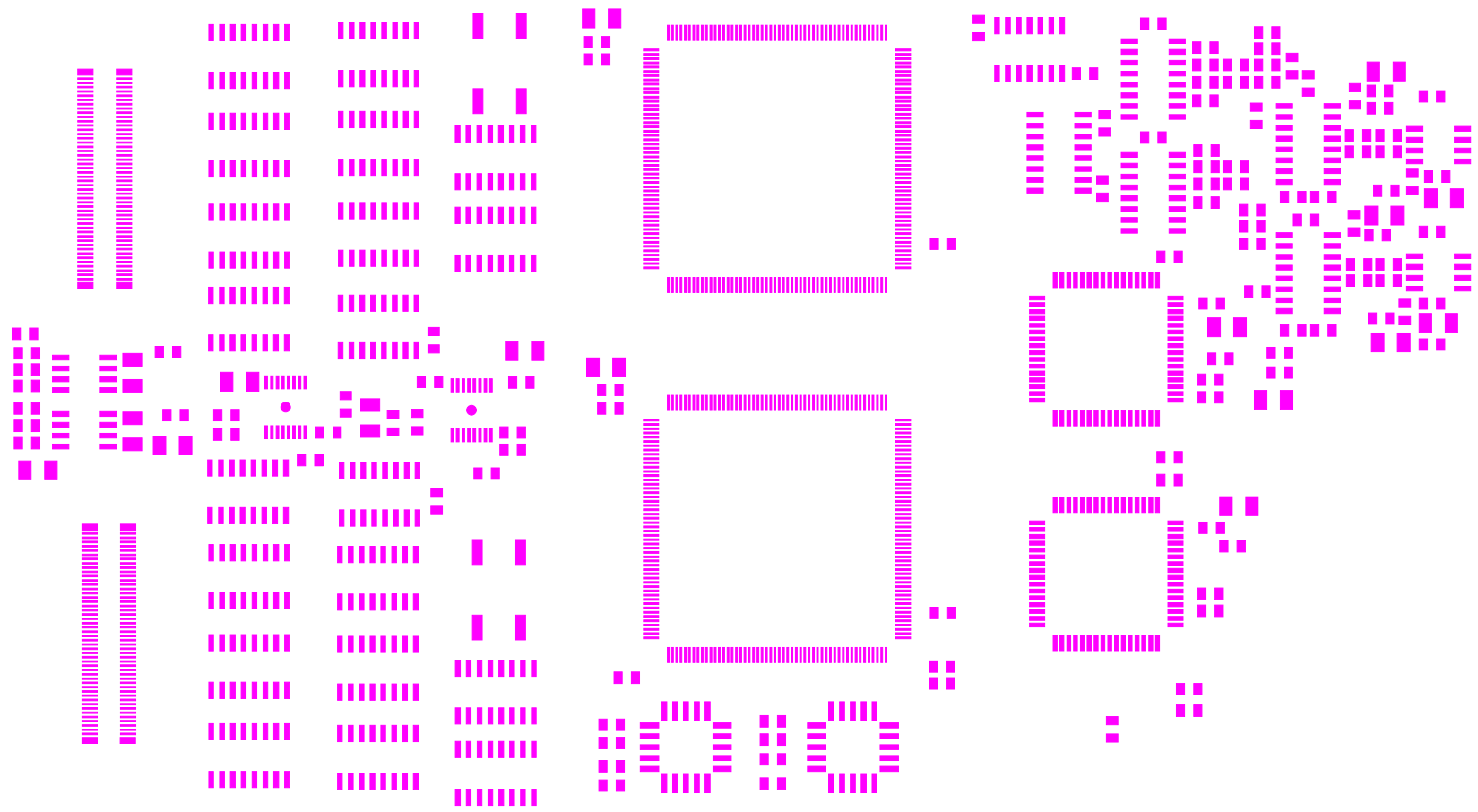




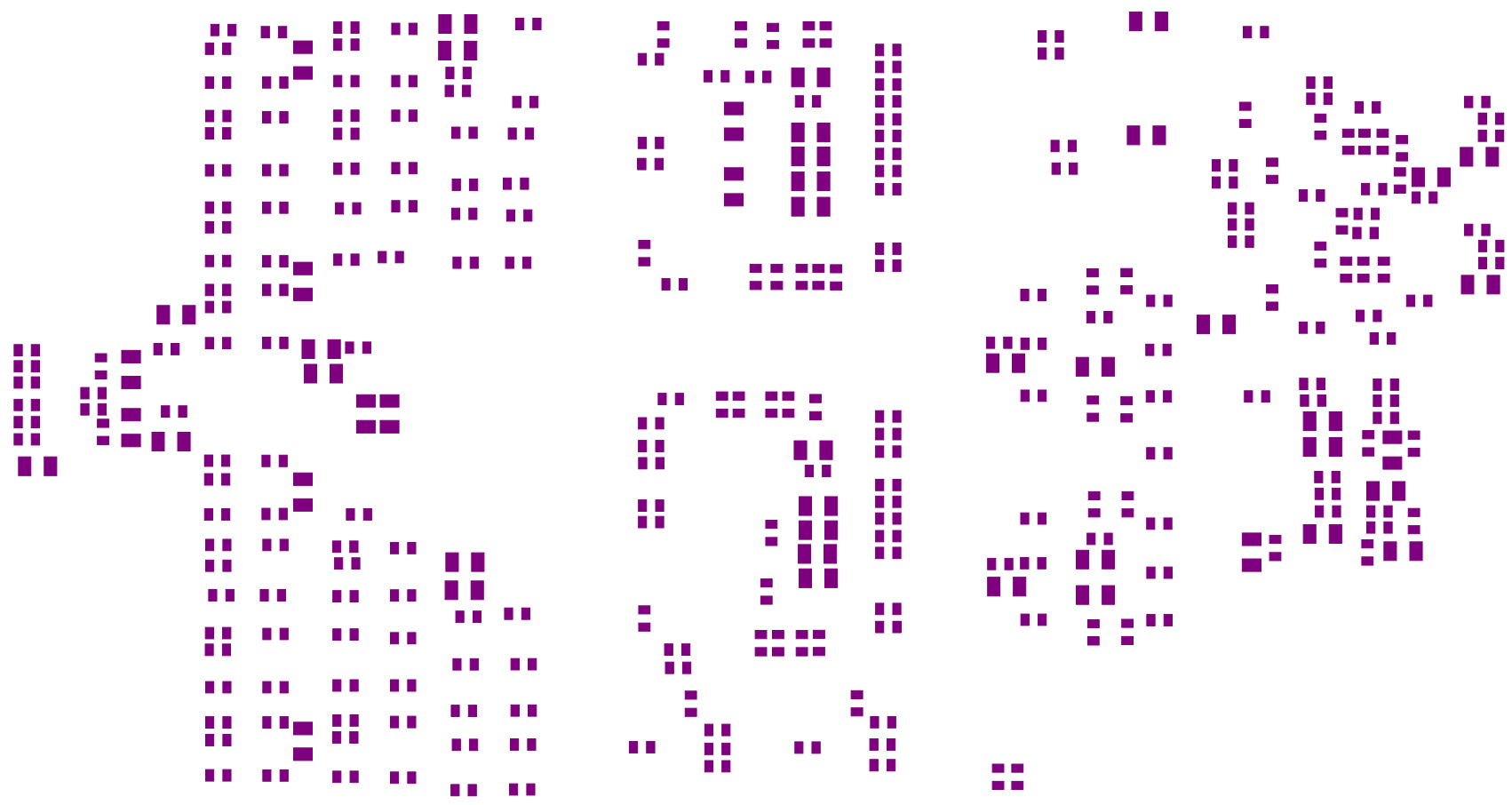
Artwork_15: Top solder mask



Artwork_16 : Bottom solder mask



Artwork_17: Top paste mask



Artwork_18 : Bottom paste mask

