B2468(V3.3) Board Size (mm)

BOARD's DRILL SCHEDULE (Inch)

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.015	1243	YES	---
⊞	.02	68	YES	---
⦶	.025	15	YES	---
⊟	.028	3	YES	---
⊖	.035	8	YES	---
◫	.041	13	YES	---
⊕	.1	10	YES	---
□	.12	4	YES	---
	.14	4	NO	---

BOARD SPECIFICATIONS

1. Board Layers: 12
2. Layer Stack Order:

Layer1 (Artwork_1):	Top component layer (Signal_1), 0.5oz, Tz=50 ohm
Layer2 (Artwork_2):	Power_2 (VCC18A), 1oz
Layer3 (Artwork_3):	Inner signal layer (Signal_2), 0.5oz, Tz=50 ohm.
Layer4 (Artwork_4):	Inner signal layer (Signal_3), 0.5oz, Tz=50 ohm
Layer5 (Artwork_5):	Power_4 (VDD), 1oz
Layer6 (Artwork_6):	Power_1 (GROUND), 1oz
Layer7 (Artwork_7):	Splited AGND plane (AGNDA, AGNDB), 1oz
Layer8 (Artwork_8):	Splited power plane (VCC30A, VCC30B), 1oz
Layer9 (Artwork_9):	Inner signal layer (Signal_4), 0.5oz, Tz=50 ohm
Layer10 (Artwork_10):	Inner signal layer (signal_5), 0.5oz, Tz=50 ohm
Layer11 (Artwork_11):	Power_3 (VCC18B), 1oz
Layer12 (Artwork_12):	Bottom component layer (signal_6), 0.5oz, Tz=50 ohm

3. Apply solder mask over bare copper on both side:
   - Artwork_13: Top silkscreen.
   - Artwork_14: Bottom silkscreen
4. Apply silkscreen on both side:
   - Artwork_15: Top solder mask
   - Artwork_16: Bottom solde mask
5. Material: FR4 with Tg >= 170C
6. Board thickness: 0.070'' +/- 0.010.
7. TRACE IMPEDENCE: 50 ohms +/- 10%.
8. See attached page for layer thickness specifications
9. Copper thickness 1oz before plating for all the power planes.
10. Copper thickness 0.5oz before plating for all the signal layers.
11. Ni/Au plating (3 to 8 micro-inches soft gold) over bare copper
12. All layers mininum trace width/clearence 0.007"/0.007"
13. All dimensions are in inches unless otherwise noted.

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SCHM# B2467V3.3
SPEC# B2468V3.3
ASSM# B2469V3.3

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
B2468 Specification

SHEET 1 OF 1
DATE 11/26/2001
DRAWN TANG

B- 2468
REV 3.3