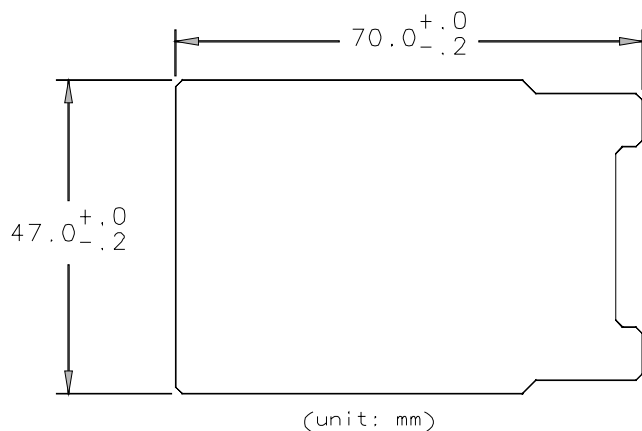


B-2382 V3.2C Specification Drawing



BOARD's DRILL SCHEDULE (unit: inch)

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.015	228	YES	---
⊞	.02	2	YES	---
⊕	.028	3	YES	---
⊞	.035	46	YES	---
⊖	.041	6	YES	---
⊞	.059	6	YES	---

B-2382 V3.2C PC BOARD SPECIFICATIONS

- Board Layers: 8
- Layer Stack Order:
 - Layer1: Top component layer(signal_1).
 - Layer2: Power plane(Vcc, AVCC).
 - Layer3: Inner signal layer(signal_3).
 - Layer4: Power plane (AGND).
 - Layer5: Power plane (GROUND).
 - Layer6: Inner signal layer(signal_4).
 - Layer7: Power plane (VEE,VCC2).
 - Layer8: Bottom component layer(signal_2).
- Apply silkscreen on both side:
 - Film9: Top component side silkscreen.
 - Film10: Bottom component side silkscreen.
- Apply solder mask over bare copper on both side:
 - Film11: Top component side solder mask.
 - Film12: Bottom component side solder mask.
- Material: FR4.
- Board thickness: 0.062'' +/- 0.010.
- Board outline is metric
- All layers are equal thickness.
- Copper thickness 1oz before plating.
- All dimensions are in inches unless otherwise noted.

11: Contact person:

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 Electronics Development Group
 University of Chicago
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Note: Rev. v3.2c interchanges label for layer 4 and layer 5 in Item 2 (layer stack order) above.

SCHM# B-2381 v3.2c
 SPEC# B-2382 v3.2c
 ASSM# B-2383 v3.2c

UNIVERSITY OF CHICAGO
 ELECTRONICS DEVELOPMENT GROUP

TITLE
 B-2382 V3.2 Specification Drawing

SHEET 1 OF 1
 DATE 4/11/00
 DRAWN TANG

B- 2382
 REV V3.2c