

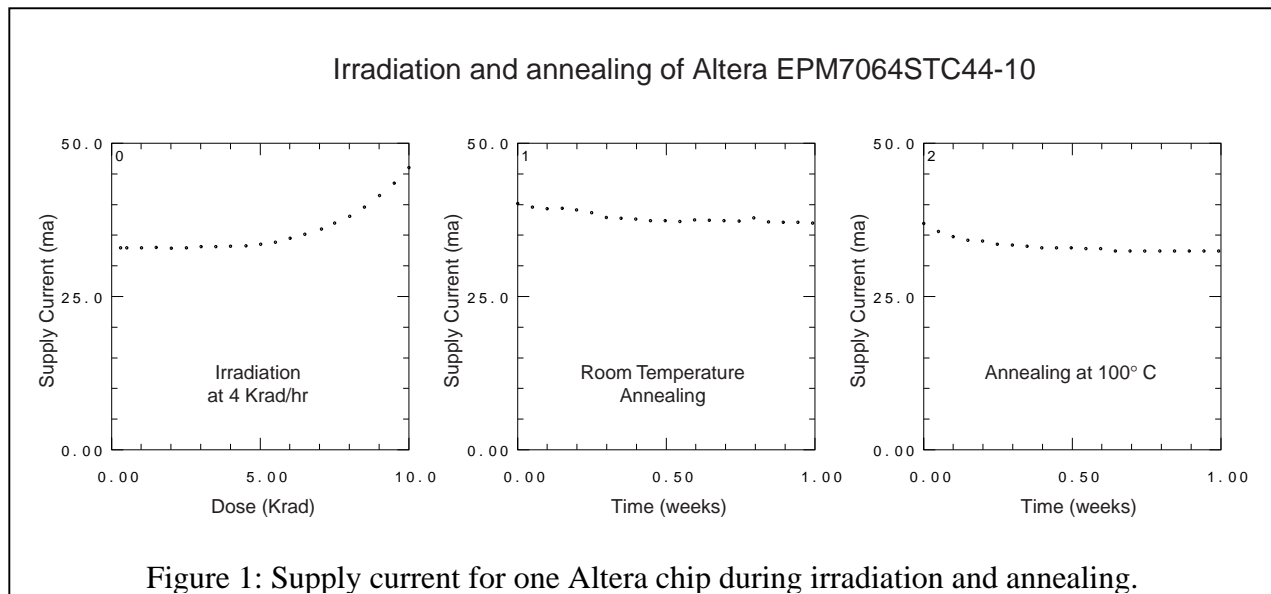
Lot Qualification of Chips for 3-in-1 Card

The TileCal 3-in-1 card contains only 2 chips which showed evidence for radiation sensitivity in tests with ionizing radiation to 50 Krad. The design requirement is 10 Krad, including a safety factor of 5 and 10 years operation at design luminosity. For this level of exposure both chips operated normally. The board was also irradiated by neutrons and no deterioration observed. It was agreed at the production readiness review that both chips would be lot qualified to 10 Krad following procedures satisfying the US ATLAS project electronics engineer.

The chips in question are the Altera EPLD, part EPM7064STC44-10, and the Exar DAC, part MP7633JS. The Altera part is a CMOS device and is a member of their MAX 7000 series. It has JTAG capability, is in a thin plastic quad flat pack (TQFP), and is of a commercial temperature grade (0 to 70 C). A batch of 12,000 chips was obtained from two diffusion lots with designations VFB2414882 and VFB2414884, both of date code BFB249925. The Exar part is a 10-bit CMOS DAC of commercial temperature grade (-40 to 85 C) in an SOIC package. A batch of 12,000 chips was obtained from lots W-11194.1 and W-11194.2, date code 9940.

For the lot qualification, it was desired to monitor the supply current to each chip during and after irradiation. This is an indicator of radiation effects. Special PC boards were constructed to allow this monitoring using computer controlled slow ADCs. Because of limitations of available equipment we tested and monitored 8 chips from each lot. This was approved by the US ATLAS project electronics engineer.

The test boards held 8 individually fused chips under power. The boards were irradiated in the Argonne Co-60 test facility at 4.1 Krad/hr to a total dose of 10 Krad. After irradiation they were returned to the lab and set up for monitoring currents during one week of annealing under power at room temperature. Several days elapsed between the end of irradiation and the start of current monitoring. After a week at room temperature, the boards were annealed at 100 C for one week. Figure 1 shows the supply current during irradiation and annealing. By the end of the process the 40% increase in current during irradiation had disappeared.



Exactly the same pattern of supply current was seen for all 16 Altera chips. For the Exar chips the supply currents were constant throughout all phases of the test. In ATLAS the dose rate is very low and the annealing process occurs continuously. Thus no increase in supply current is anticipated. Annealing is recommended as part of the test procedure in MIL-STD-883E, Method 1019.5 to account for low dose rate effects.

Following annealing, the chips were removed from the test boards. The Altera chips were inserted in a programming unit which tested the previously stored program. All chips verified as correct. Chips were then mounted in 3-in-1 cards and tested for functionality. All chips passed all tests. We conclude that the lots have been qualified for use in production. A group of 320 of the Altera chips have been provided to Barcelona, at cost, for use in the integrator ADC card.